AMENDMENTS TO THE CLAIMS

(no amendments made; claims included for convenience of examiner)

1. (Original) An apparatus for transferring signals between timing domains, comprising:
a receiver for receiving a plurality of signals operative in a first timing domain;
a decoder coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and
an output timing register coupled to the decoder for outputting the at least one decoded signal in a second timing domain.

2. (Original) The apparatus of claim 1, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

3. (Original) The apparatus of claim 1, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

4. (Original) The apparatus of claim 1, wherein the first timing domain and the second timing domain have no predetermined phase relationship.

5. (Original) An apparatus for transferring signals between timing domains, comprising:
a receiver for receiving a plurality of signals operative in a first timing domain, the receiver including a multiple-bit enabled register for each of the plurality of signals, each of the multiple-bit enabled registers being clocked using a first clock signal;
a decoder coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and
an output timing register coupled to the decoder for outputting the at least one decoded signal in a second timing domain.

6. (Original) The apparatus of claim 5, wherein the receiver further includes a first ring counter for generating a multiple-bit enable signal, each of the bits of the enable signal being used for enabling clocking of one of the bits of the multiple-bit enabled registers.

7. (Original) The apparatus of claim 6, wherein the receiver further includes a multiplexer associated with each of the multiple-bit enabled registers for selecting one of the bits from the respective multiple-bit enabled register for output to the decoder.

8. (Original) The apparatus of claim 7, wherein the receiver further includes a second ring counter for generating a multiple-bit selection signal for each multiple-bit multiplexer.

9. (Original) The apparatus of claim 8, wherein the second ring counter selects a particular bit after the first ring counter selects the particular bit and before the first ring counter selects the particular bit again.

10. (Original) The apparatus of claim 5, wherein the output timing register is clocked using a second clock signal having no phase relationship with the first clock signal.

11. (Original) An apparatus for transferring signals between timing domains, comprising:

a receiver for capturing a plurality of signals timed to a capture clock;

a decoder coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and

an output timing register coupled to the decoder for synchronizing the at least one decoded signal to a logic clock.

12. (Original) The apparatus of claim 11, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

13. (Original) The apparatus of claim 11, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

14. (Original) The apparatus of claim 11, wherein the capture clock and the logic clock have no predetermined phase relationship.

15. (Original) An apparatus for transferring signals between timing domains, comprising:

a FIFO synchronizer having a front end and a back end, wherein the front end is for capturing a plurality of signals operative in a first timing domain, and the back end is for synchronizing at least one decoded signal to a second timing domain; and

a decoder coupled between the front and back ends of the FIFO synchronizer, the decoder for decoding the captured signals to generate the at least one decoded signal.

16. (Original) The apparatus of claim 15, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

17. (Original) The apparatus of claim 15, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

18. (Original) The apparatus of claim 15, wherein the front end of the FIFO synchronizer includes a multiple-bit enabled register for capturing each of the plurality of signals.

19. (Original) The apparatus of claim 18, wherein the front end of the FIFO synchronizer further includes a first ring counter for enabling each bit of the multiple-bit enabled register.

20. (Original) The apparatus of claim 19, wherein the front end of the FIFO synchronizer further includes a multiplexer associated with each multiple-bit enabled register for selecting one of the bits from the respective multiple-bit enabled register for output to the decoder.

21. (Original) The apparatus of claim 20, wherein the front end of the FIFO synchronizer further includes a second ring counter for generating a selection signal for each multiplexer.

22. (Original) An integrated circuit device having a sending clock domain and a receiving clock domain, comprising:

a receiver for receiving a plurality of command signals operative in the sending clock domain;

a decoder coupled to the receiver for at least partially decoding the command signals to generate at least one decoded command signal; and

an output timing register coupled to the decoder for outputting the at least one decoded command signal in the receiving clock domain.

23. (Original) The integrated circuit device of claim 22, further comprising a DRAM array.

24. (Original) The integrated circuit device of claim 23, wherein the plurality of command signals command a DRAM operation which is selected from the group of DRAM operations consisting of a read operation, a write operation and a refresh operation.

25. (Original) The integrated circuit device of claim 22, wherein the sending clock domain and the receiving clock domain have no predetermined phase relationship.

26. (Original) An integrated circuit device having a sending clock domain and a receiving clock domain, comprising:

a receiver for receiving a plurality of command signals operative in the sending clock domain and for receiving an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the circuit device is not enabled;

a decoder coupled to the receiver for at least partially decoding the command signals to generate at least one decoded command signal if the circuit device is enabled; and

an output timing register coupled to the decoder for outputting the at least one decoded command signal in the receiving clock domain if the circuit device is enabled.

27. (Original) The integrated circuit device of claim 26, wherein the decoder inhibits decoding of the command signals if the circuit device is not enabled.

28. (Original) The integrated circuit device of claim 26, wherein the output of the at least one decoded command signal is inhibited if the circuit device is not enabled.

29. (Original) The integrated circuit device of claim 26, wherein the enable signal is a chip select signal.

30. (Original) An apparatus for transferring signals between timing domains, comprising:

means for receiving a plurality of signals operative in a first timing domain;

means for at least partially decoding the signals to generate at least one decoded signal; and

means for outputting the at least one decoded signal in a second timing domain.

31. (Original) The apparatus of claim 30, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

32. (Original) The apparatus of claim 30, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

33. (Original) A method of transferring signals between timing domains of a digital circuit, comprising:

receiving a plurality of signals operative in a first timing domain;

at least partially decoding the signals to generate at least one decoded signal; and

outputting the at least one decoded signal in a second timing domain.

34. (Original) The method of claim 33, wherein receiving the plurality of signals includes receiving command signals, and at least partially decoding the signals includes generating at least one decoded command signal.

35. (Original) The method of claim 33, wherein receiving the plurality of signals includes receiving address signals, and at least partially decoding the signals includes generating at least one decoded address signal.

36. (Original) The method of claim 33, wherein the first timing domain and the second timing domain have no predetermined phase relationship.

37. (Original) A method of transferring signals between timing domains of a digital circuit, comprising:

capturing a plurality of signals timed to a capture clock of the digital circuit;
at least partially decoding the signals to generate at least one decoded signal; and
synchronizing the at least one decoded signal to a logic clock of the digital circuit.

38. (Original) The method of claim 37, wherein capturing the plurality of signals includes capturing command signals, and at least partially decoding the signals includes generating at least one decoded command signal.

39. (Original) The method of claim 37, wherein capturing the plurality of signals includes capturing address signals, and at least partially decoding the signals includes generating at least one decoded address signal.

40. (Original) The method of claim 37, wherein the capture clock and the logic clock have no predetermined phase relationship.

41. (Original) A method of transferring signals between timing domains of a digital circuit using a first-in first-out (FIFO) synchronizer having a front end and a back end, comprising:

capturing a plurality of signals operative in a first timing domain at the front end of the FIFO synchronizer;
transferring the signals from the front end of the FIFO synchronizer to a decoder;
decoding the signals at the decoder to generate at least one decoded signal;

transferring the at least one decoded signal to the back end of the FIFO synchronizer; and

synchronizing the at least one decoded signal to a second timing domain at the back end of the FIFO synchronizer.

42. (Original) The method of claim 41, wherein capturing the signals includes capturing command signals, and decoding the signals includes generating at least one decoded command signal.

43. (Original) The method of claim 41, wherein capturing the signals includes capturing address signals, and decoding the signals includes generating at least one decoded address signal.

44. (Original) The method of claim 41, wherein capturing the signals includes clocking each signal into a multiple-bit enabled register using a first clock signal.

45. (Original) The method of claim 44, wherein synchronizing the at least one decoded signal includes inputting the at least decoded signal to an output timing register clocked using a second clock signal with no predetermined phase relationship with the first clock signal.

46. (Original) A method of transferring command signals between a sending clock domain and a receiving clock domain of an integrated circuit device, comprising:

receiving a plurality of command signals operative in the sending clock domain of the integrated circuit device;

at least partially decoding the command signals to generate at least one decoded command signal; and

outputting the at least one decoded command signal in the receiving clock domain of the integrated circuit device.

47. (Original) The method of claim 46, wherein the integrated circuit device includes a dynamic random access memory (DRAM).

48. (Original) The method of claim 47, wherein receiving the command signals includes receiving signals that command a DRAM operation selected from the group of DRAM operations consisting of a read operation, a write operation and a refresh operation.

49. (Original) The method of claim 46, wherein the sending clock domain and the receiving clock domain have no predetermined phase relationship.

50. (Original) A method of transferring command signals between a sending clock domain and a receiving clock domain of an integrated circuit device, comprising:

receiving a plurality of command signals operative in the sending clock domain of the integrated circuit device;

receiving an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the integrated circuit device is not enabled; and

if the enable signal indicates that the integrated circuit device is enabled, decoding the command signals to generate at least one decoded command signal and outputting the at least one decoded command signal in the receiving clock domain of the circuit device.

51. (Original) The method of claim 50, further comprising, if the enable signal indicates that the integrated circuit device is not enabled, inhibiting decoding of the command signals.

52. (Original) The method of claim 50, further comprising, if the enable signal indicates that the integrated circuit device is not enabled, inhibiting outputting of the at least one decoded command signal.

53. (Original) The method of claim 50, wherein the enable signal is a chip select signal.